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University of California, Santa Barbara and NEC Labs America, Princeton*

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Outline



- Motivation
- An Overview of Our Approach

2 Technical Details

- Summarization
- Assertion Checking

3 Experiments





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Motivation

 Increasing interest in web-based business management involving inter-organizational interactions and critical transactions



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- Web services provide mechanisms implementing such applications



Introduction Motivation

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- Web services provide mechanisms implementing such applications
- Need formal mechanisms to ensure that web services behave properly



Introduction Motivation

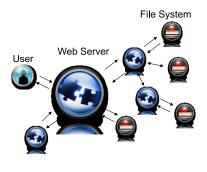
Motivation

- Increasing interest in web-based business management involving inter-organizational interactions and critical transactions
- Web services provide mechanisms implementing such applications
- Need formal mechanisms to ensure that web services behave properly
- We propose an automatic verification tool featuring efficient symbolic encoding and modular verification using summarization



Web Services

- Interoperable Machine to Machine software
- Some Industry Standards: Business Process Execution Language (BPEL), Web Service Description Language (WSDL)

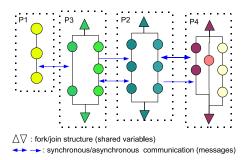




An Overview of Our Approach

BPEL Web Services

A distributed system with both multi-threading (internal) and message-passing (external).



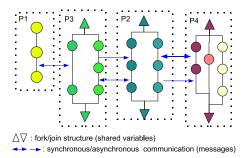


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■ *flow* activities ⇒ fork/join structure



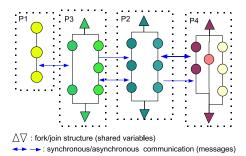


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BPEL Web Services

A distributed system with both multi-threading (internal) and message-passing (external).

- flow activities \Rightarrow fork/join structure
- *invoke, receive, reply* activities ⇒ asynchronous/synchronous communications



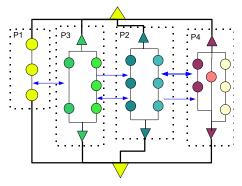


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An Overview of Our Approach

Monolithic Analysis

- Consider all of them as one composite service by adding a outer fork/join structure
- Need to consider all interleavings among threads
- Suffer from state explosion problem



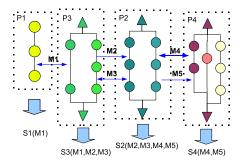
Introduction

An Overview of Our Approach

Modular Verification

From processes to summaries.

- Interference among processes is limited to the values of messages
- Summarize processes on messages



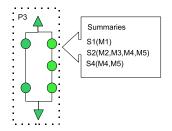


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An Overview of Our Approach

Modular Verification

 Modular Analysis: check one process within which interactions among other processes are patched by their summaries

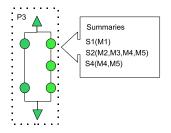




An Overview of Our Approach

Modular Verification

- Modular Analysis: check one process within which interactions among other processes are patched by their summaries
- From $P_1 \times \ldots \times P_n$ to $P_1 + \ldots + P_n$

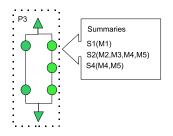




An Overview of Our Approach

Modular Verification

- Modular Analysis: check one process within which interactions among other processes are patched by their summaries
- From $P_1 \times \ldots \times P_n$ to $P_1 + \ldots + P_n$
- No precision loss with respect to assertion checking within processes



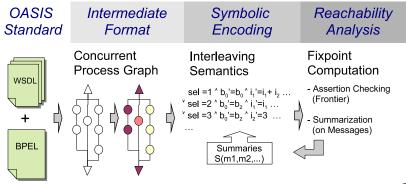


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Introduction

An Overview of Our Approach

Our Framework





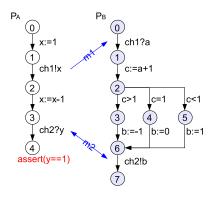
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- Technical Details
 - Summarization

Summarization: A Simple Example

Consider the following two concurrent processes.

- \blacksquare P_A invokes P_B
- An assertion within P_A at node 4





Summarization

Summarize Process Behavior

A relation among input and output messages



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Summarize Process Behavior

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Encode each send activity $(ch_i!x)$ as an assignment to a message $(m'_i = x)$



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A relation among input and output messages

- Encode each send activity (ch_i!x) as an assignment to a message (m'_i = x)
- Encode each receive activity $(ch_i?x)$ as an assignment to a variable $(x' = m_i)$



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Summarize Process Behavior

A relation among input and output messages

- Encode each send activity (ch_i!x) as an assignment to a message (m'_i = x)
- Encode each receive activity (ch_i?x) as an assignment to a variable (x' = m_i)
- Compute the forward fixpoint of reachable states



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Summarize Process Behavior

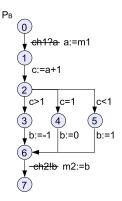
A relation among input and output messages

- Encode each send activity (ch_i!x) as an assignment to a message (m'_i = x)
- Encode each receive activity (ch_i?x) as an assignment to a variable (x' = m_i)
- Compute the forward fixpoint of reachable states
- Project the fixpoint to input and output messages (using existential quantifier elimination)



Summarization

Summarize Process Behavior: A Simple Example



The summary of P_B is:

$$\begin{array}{l} (m_1 > 0 \land m_2 = 1) \lor \\ (m_1 = 0 \land m_2 = 0) \lor \\ (m_1 < 0 \land m_2 = -1) \end{array}$$

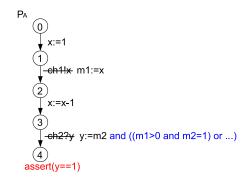


Technical Details

Summarization

Compose Summaries: A Simple Example

 Compose summaries by conjoining the summaries of other processes with the receive activities



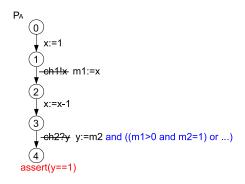


Technical Details

Summarization

Compose Summaries: A Simple Example

- Compose summaries by conjoining the summaries of other processes with the receive activities
- One can prove P_A 's assertion modularly





- Technical Details
- Summarization

Modularity of Processes

An assertion can be proven via modular analysis if and only if it can be proven via monolithic analysis.

T: transition relation, I: initial states, X: variables
reach(T, I) returns the fixpoint of reachable states
The insight comes from the property:

 $reach(T, I(C) \land I(X)) \equiv I(C) \land reach(T, I(X))$

if $C \subseteq X$ are parameterized constants (not defined in T).



- Technical Details
 - Summarization

Modularity of Processes

From the receiver's perspective, a message is a parameterized constant



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- One can summarize the receiver's behavior (reach(T, I(X))) without knowing the states of its input messages (I(C))



- Technical Details
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Modularity of Processes

- From the receiver's perspective, a message is a parameterized constant
- One can summarize the receiver's behavior (reach(T, I(X))) without knowing the states of its input messages (I(C))
- One can compute the precise reachable states of the receiver's output messages $(reach(T, I(C) \land I(X)))$ by conjoining
 - the states of the receiver's input messages (I(C)) and
 - the receiver's summary (reach(T, I(X)))

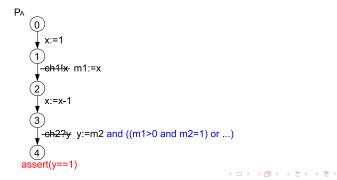


Technical Details

Summarization

Modularity of Processes: A Simple Example

The state of m₁ is initialized upon sending and is imposed implicitly after sending



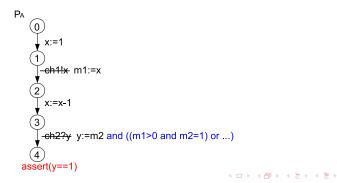


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Modularity of Processes: A Simple Example

- The state of m₁ is initialized upon sending and is imposed implicitly after sending
- The summary of *P*_B (the relation among *m*₁ and *m*₂) is conjoined upon receiving



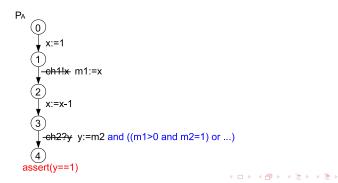


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Summarization

Modularity of Processes: A Simple Example

- The state of m₁ is initialized upon sending and is imposed implicitly after sending
- The summary of P_B (the relation among m₁ and m₂) is conjoined upon receiving
- P_A gets the precise reachable states of m_2 ($m_2 = 1$).





Summarization

Restrictions

- We assume that each channel is associated with precisely one send activity and one receive activity
- The examples we analyzed do not violate this condition
- For the specifications which violate this condition:
 - Rename channels if multiple send/receive pairs use the same channel
 - If there is a send or receive activity within a loop, unwind the loop a fixed number of times



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Assertion Checking

Efficient Assertion Checking

Use frontier, the new states reachable from the previous iteration, to detect violation and convergency



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Assertion violated at the i^{th} iteration when $F^i \cap Err \neq \emptyset$



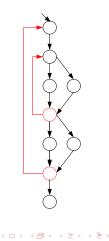
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Technical Details

Assertion Checking

Termination Condition

- When the CPG is acyclic,
 - No back edges
 - Terminate when Fⁱ is empty



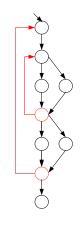


Technical Details

Assertion Checking

Termination Condition

- When the CPG is acyclic,
 - No back edges
 - Terminate when Fⁱ is empty
- When the CPG is not acyclic,
 - Compute S_{back}, the states associated with the source nodes of the back edges (much smaller than the universe)
 - At each iteration, compute *R*_{back}, the set of reached states fall in *S*_{back}
 - Terminate when $F^i \setminus R_{back}$ is empty



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Technical Details

-Assertion Checking

The Assertion Checking Algorithm

Reach_frontier(T,I,Err, S_{back})

- F = I;
- $\blacksquare R_{back} = I \cap S_{back};$

false - assertion violated. true - assertion proven.



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RETURN true;

false - assertion violated. true - assertion proven.



Experiments

Experiment: Loan Approval

	Monolithic Verification	Modular Verification						
	All	Approval	Assessor	Approver	Customer			
Result	Р	Р	S	S	S			
Time (s)	1227.2	124.5	0.1	0.1	0.1			
Memory (MB)	810	490	289	290	290			
ITRs	32	16	10	10	5			

- Customer invokes Approval which invokes Assessor and Approver
- Result: NA-did not terminate, P-passed assertion checks, S-summarized
- ITRs: the number of iterations of the fixpoint computation



Experiments

Experiment: Travel Agency

	Monolithic Verification	Modular Verification			
	All	VTA	Hotel	Flight	User
Result	NA	Р	S	S	S
Time (s)	18947	814	13.5	13.4	34.6
Memory (MB)	1663	363	273	363	284
ITRs	57	55	23	22	30

- User invokes VTA which invokes Hotel and Flight
- Result: NA-did not terminate, P-passed assertion checks, S-summarized
- ITRs: the number of iterations of the fixpoint computation



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Conclusion

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Conclusion

- We propose an automatic symbolic model checker for concurrent systems having multi-threading and message-passing
- We propose modular verification for message-passing processes to achieve scalability
- We propose an efficient symbolic encoding and reachability analysis to facilitate our approach
- We have implemented a prototype tool that can automatically analyze web services specified in BPEL+WSDL



Related Work

- BPEL Verification:
 - Safety property [Foster et al. ICWS04] [Lohmannet et al. BPM06]
 - LTL property [Fu et al. WWW04] [Nakajima ENTCS06]
 - Timed CTL property [Qiu et al. ISFM05]



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- Compositional Reasoning:
 - LTSA [Cobleigh et al. TACAS03]
 - Magic/Comfort [Chaki et al. FMSD04] [Sharygina et al. CAV05]



Thank you. Any Questions?